NM Institute Of Engineering and Technology, Bhubaneswar

DEPARTMENT:CSE

LESSON PLAN: Academic Year 2022-23 (Odd Semester) COURSE: DIPLOMA SEMESTER: 3rd

Subject/Code: COMPUTER SYSTEM ARCHITECTURE Faculty Name: Swarnalata Rath

Sl. No.	Name of the Topic to Cover	Text Book	Teaching Method	Course Progress	Remark
1	Basic Structure of computer hardware	T1	P	100%	
2	Functional Units of Computer	T2	G	100%	
3	Computer components	T2	P	100%	
4	Performance measures	T3	G	100%	
5	Memory addressing & Operations	T1	G	120%	
6	Main Memory, Secondary storage, Cache memory.	T1	G	99%	
7	Addressing modes & Instruction Sequencing	T2	G	100%	
8	Execution cycle, Hardwired control, Micro programmed control.	T2	G	100%	
9	Fundamentals to instructions	T1	G	100%	
10	Multiplication of signed and unsigned numbers	T2	P	100%	
11	Booth Multiplier, Array Multiplier	T1	G	98%	
12	Integer Division	T1	P	100%	
13	Floating- point Numbers and operations.	T2	G	100%	
14	Microprocessors, Instruction set	T3	G	100%	
15	Assembly Language Programmimg Stack	T1	G	99%	
16	Operands with instructionm set	T2	G	100%	
17	Op Codes with instruction set format	T2	P	100%	
18	Instruction formats	T1	G	100%	
19	Addressing Modes	T2	G	100%	
20	Flow control and Error control	T1	G	99%	
21	Subroutine, Interrupt, Accessing I/O devices	T2	G	98%	
22	Standard I/O Interfaces- RS-232C	T3	P	100%	
23	IEEE-488, USB, Data Transfer techniques	T2	G	100%	
24	Modes of Data Transfer	T1	G	100%	
25	Register Files	T3	G	100%	
26	Register Transfer: Register Transfer Language, Register Transfer	T2	G	100%	
27	Bus and Memory Transfers	T2	P	100%	
28	Control Unit: Control Memory	T1	P	99%	
29	Micro program Example, Design of Control Unit	T2	G	100%	
30	Data Transfer and Manipulation, Program Control.	T1	G	100%	
31	Instruction Set Architecture Design, A simple Instruction Set Architecture	T2	G	100%	
32	Logic Micro operations, Shift Micro operations.	T2	G	100%	
33	Arithmetic Micro operations	T3	G	99%	
34	Address Sequencing	T3	P	100%	
35	MemoryOrganization: Memory Hierarchy, Main Memory.	T1	P	99%	
36	Auxiliary Memory, Associative Memory	T2	G	100%	
37	Cache Memory with example	T3	G	100%	

38	Cache Mapping Techniques	T3	G	100%	
39	Mapping techniques with problems	T2	P	100%	
40	Virtual Memory	T2	P	100%	
41	Virtual Mapping techniques with problems	T3	G	98%	
42	Bus Structure	T2	G	100%	
43	Bus and System Bus	T1	G	100%	
44	SCSI & USB	T2	G	100%	
45	Single Bus vs Multiple Bus	T3	P	100%	
46	Bus and Memory Transfers	T3	P	99%	
47	Parallel Processing	T2	G	100%	
48	Pipelining	T1	P	99%	
49	Arithmetic Pipeline, Instruction Pipeline.	T3	P	100%	
50	Linear Pipeline	T3	G	100%	
51	Multiprocessor	T2	P	100%	
52	Flynn"s Classification	T2	P	100%	
53	SISD,SIMD,MISD,MIMD	T3	G	99%	
54	Basic Parameters of Bus design	T3	P	100%	
55	Multiprocessors: Characteristics of Multiprocessors, Interconnection Structures	T2	P	100%	
56	RISC vs CISC	T2	G	98%	
57	Inter Processor Communication, And Synchronization	T3	P	99%	
58	Input/output Organization: Input-Output Interface.	T3	P	100%	
59	Interrupt driven I/O	T2	G	100%	
60	Array & vector processor	T2	G	99%	

Method of Teaching
G: Green Board Teaching
P: Power Point Teaching

Faculty Signature: Swarnalata Rath

At the end of this course, students will be able to:

Understand the basic structure of a computer with instructions.

Learn about machine instructions and program execution

Learn about the internal functional units of a processor and how they are interconnected

Understand how I/O transfer is performed

Learn about basic memory circuit, organization and secondary storage.

Understand concept of parallel processing

TEXT BOOKS:

Moris Mano,"Computer System Architecture",PHI

Er. Rajeev Chopra,"Computer Architecture and Organization",S.Chand

Parthasarthy, Senthil Kumar"Fundamentals of Computer Architecture",TMH